ABSTRACT

A signal processing apparatus for assigning channels to a plurality of DSP's to be used comprises a control circuit for controlling the DSP's, a library for storing a plurality of signal processing algorithms, and a channel assignment table. The control circuit, when an assignment designation of a channel and an algorithm for each of the DSP's is received, compares the designated algorithm with the algorithms having been already downloaded to the DSP's based on the table, thereby downloading only an algorithm required to be newly downloaded from the library to the DSP's or between the DSP's and assigning the downloaded algorithm to the received channel. The channel assignment table can fixedly/variably store a relationship between processing positions (time slots) in addition to the relationship between the channels and the DSP's. In the presence of an empty processing position in a DSP, the algorithm is newly downloaded from the concerned DSP, while in the absence of an empty processing position in a DSP, the algorithm is downloaded from another DSP, and then the table is updated.